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Evaluation of Lower Resolution ADCs with Konverter

Overview

Intersil offers several families of pin-compatible ADCs operating up to 500MSPS with resolutions from 8 to 16 bits. In some cases, ADC evaluation daughter cards are only produced for the highest speed grade and the highest resolution. These boards were designed to also be used at a lower sample rate or a lower resolution to support evaluation of the full range of Intersil ADCs.

Evaluation Options

The maximum speed grade ADC can always be operated at a lower sample rate. Slower speed grade parts are based on the same ADC core but are not tested beyond their specified maximum sample rate. Typically, lower sample rates result in improved dynamic performance as shown in the datasheet for each ADC.

Similarly, the number of output bits may be truncated by the Konverter software to emulate the performance of a lower resolution ADC.

Table 1 indicates higher resolution ADC evaluation boards that should be used to evaluate lower resolution ADCs.

TABLE 1.

TO EVALUATE THIS ADC (Note 1)	USE THIS BOARD
KAD5610P-nnQ72 (Note 2)	KDC5612EVAL
KAD5510P-nnQ48	KDC5512-Q48EVAL
KAD5510P-50Q72	KDC5512-50EVALZ
ISLA212PnnIRZ (Note 3)	ISLA214IR72EV1Z
ISLA212P50IRZ	ISLA214P50IR72EV1Z
ISLA222PnnIRZ	ISLA224IR72EV1Z

NOTES:

1. The nn refers to the speed grade; Q48 and Q72 refer to the package option.
2. For KAD part numbers 55 = single and 56 = dual; the next two digits (10|12) are the number of bits.
3. For ISLA part numbers, the second digit refers to the number of channels: 1 = single, 2 = dual; the third digit is the number of bits: 2 = 12-bit, 4 = 14-bit

See the Ordering Guide section on the High Speed ADC Evaluation Platform web page for up-to-date evaluation board compatibility information.

SNR Impact

The Signal to Noise Ratio (SNR) for pipeline ADCs is set by the input stage thermal noise, clock jitter, DNL noise (higher order harmonics) and digital output quantization noise. Combining these four factors with a root sum of squares gives the total noise voltage as shown in Equation 1.

$$V_{NOISE} = \sqrt{Thermal^2 + Quantization^2 + DNL^2 + Jitter^2} \quad \text{(EQ. 1)}$$

The SNR in dB can then be calculated using Equation 2.

$$SNR = 20 \times \log(V_{SIGNAL}/V_{NOISE}) \quad \text{(EQ. 2)}$$

When there are enough output bits to minimize the impact of quantization noise, typically the thermal noise will dominate. If the number of output bits is reduced, the quantization noise will increase, allowing it to dominate the SNR. The following illustration will show how the increase in quantization noise from 12 bits to 10 bits decreases a 12-bit ADC's SNR.

The SNR due to quantization noise for a given number of digital output bits (numbits) may be calculated with Equation 3:

$$SNR = (6.02 \times numbits) + 1.76 \quad \text{(EQ. 3)}$$

For 12 bits:

$$SNR = (6.02 \times 12) + 1.76 = 74dB \quad \text{(EQ. 4)}$$

For 10 bits:

$$SNR = (6.02 \times 10) + 1.76 = 61.96dB \quad \text{(EQ. 5)}$$

The increase in quantization noise reduces the ADC's SNR and can be clearly seen when evaluating a 12-bit ADC like the KAD5512P-50 in 10-bit mode. The typical SNR will be reduced from 65.9dB (thermal limited) to 60.7dB (quantization limited), about 1dB less than the maximum possible quantization-limited SNR of 61.96dB for a 10-bit output.

SFDR Impact

Reducing the number of output bits from 12 to 10 will also degrade the linearity slightly. The overall SFDR will not change much, but additional higher order harmonics will begin to show up in the noise floor.

Power Impact

The Konverter software dynamically reports the power consumed by the ADC being tested. This value will not change when using a 12-bit ADC to evaluate the performance of a 10-bit ADC because all the output bits are still active. Please refer to the ADC datasheet power specifications to compare 12-bit and 10-bit power dissipation.

Example

The KDC5512-50EVALZ evaluation board may used in the evaluation of the KAD5512P-50Q72 and KAD5510P-50Q72. In both cases, this board is populated with the KAD5512P-50Q72. The KAD5510P-50Q72 operation can be evaluated with the KAD5512P-50Q72 by only observing the ten most significant bits of the twelve bit output. This application note describes the necessary settings in the Konverter software to perform this task.

Configuring the Konverter Software

Proceed with hardware and software installation as described in AN1433 and AN1434. After the system is running, the captured data resolution may be changed. In order to use a 12-bit ADC to evaluate the performance of the 10-bit version, select "Conditions" from the "Setup" menu as shown in Figure 1.

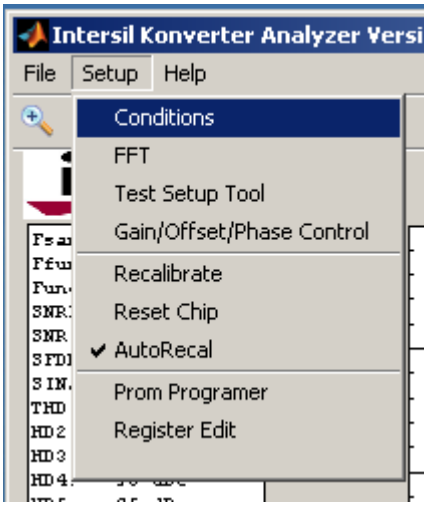

FIGURE 1. ACCESSING THE CONDITIONS DIALOG

In the Conditions dialog box change the "Number of Bits" from 12 to 10 as shown in Figure 2.

The results of this change can be seen by comparing the FFT plots in Figure 3 and Figure 4. Note that the SNR in the 12-bit example (Figure 3) is 66dBFS and in the 10-bit case (Figure 4) it decreases to 60.8dBFS. The SFDR is not directly impacted but there are additional spurs below the level of the worst harmonic. These spurs can further degrade the SNR in some cases. If this is an issue, the pin-compatible KAD5512P-50Q72 can always be used to replace the KAD5510P-50Q72 provided the two additional least significant bits (LSBs) are routed on the PCB.

The 12-bit performance of the ISLA212P212P50IRZ may be verified using the 14-bit ISLA214P50IRZ by changing the default number of bits from 14 to 12.

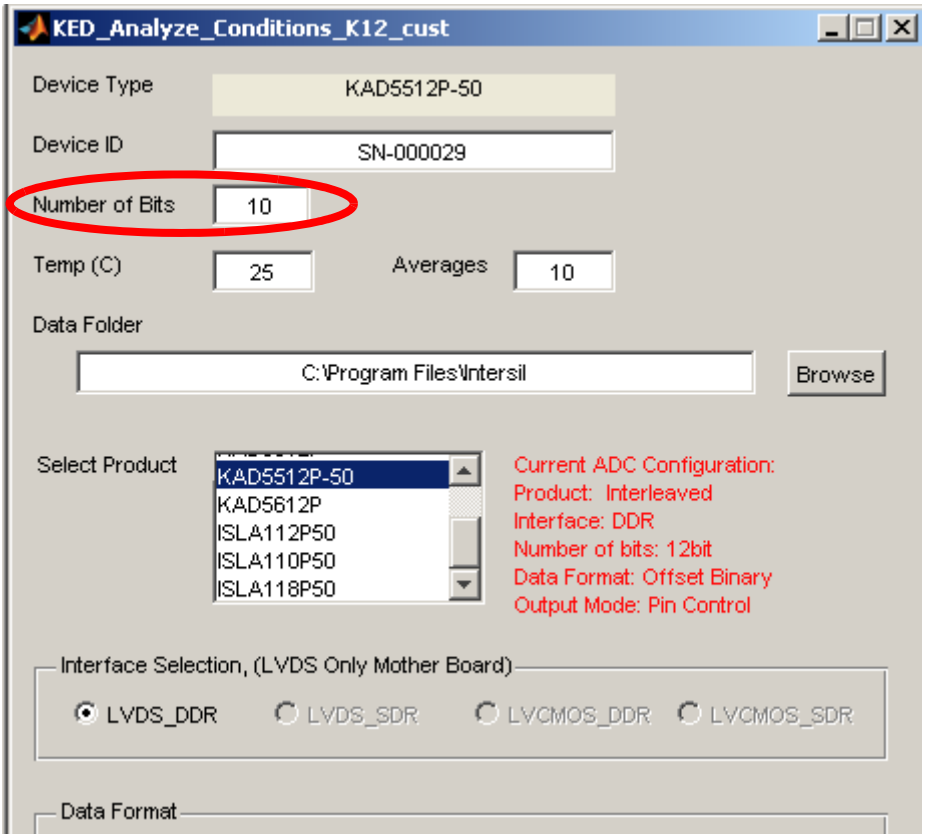

FIGURE 2. CHANGING THE NUMBER OF BITS

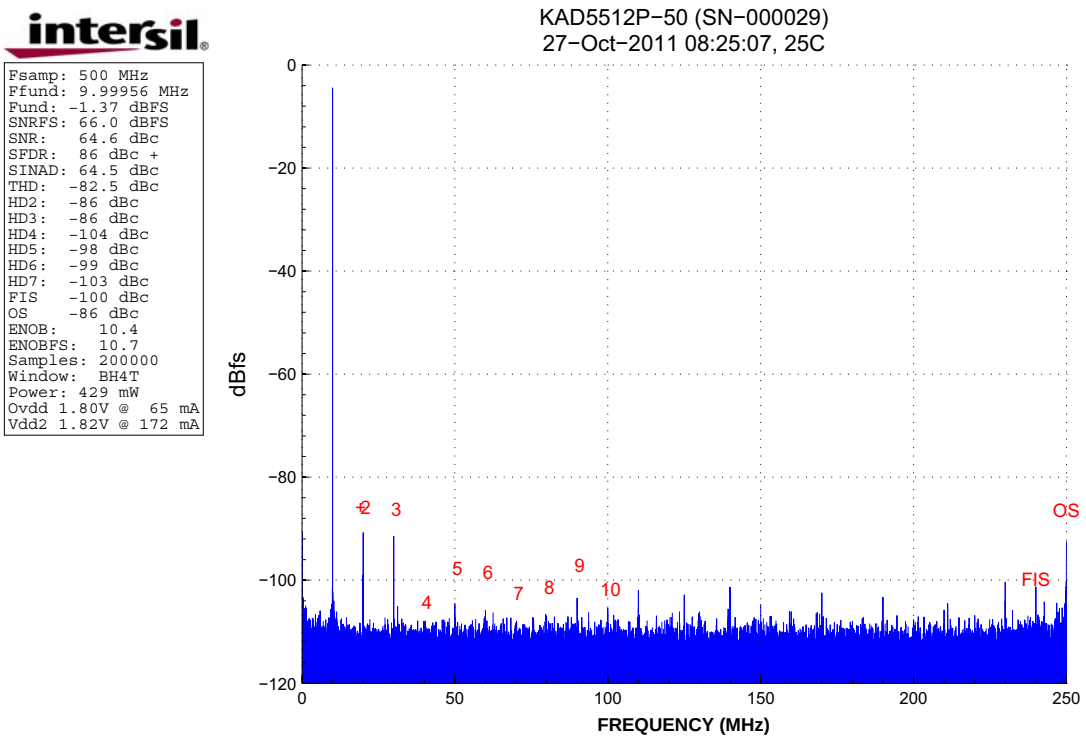

FIGURE 3. KAD5512P-50Q72 IN 12-BIT OUTPUT MODE (DEFAULT)

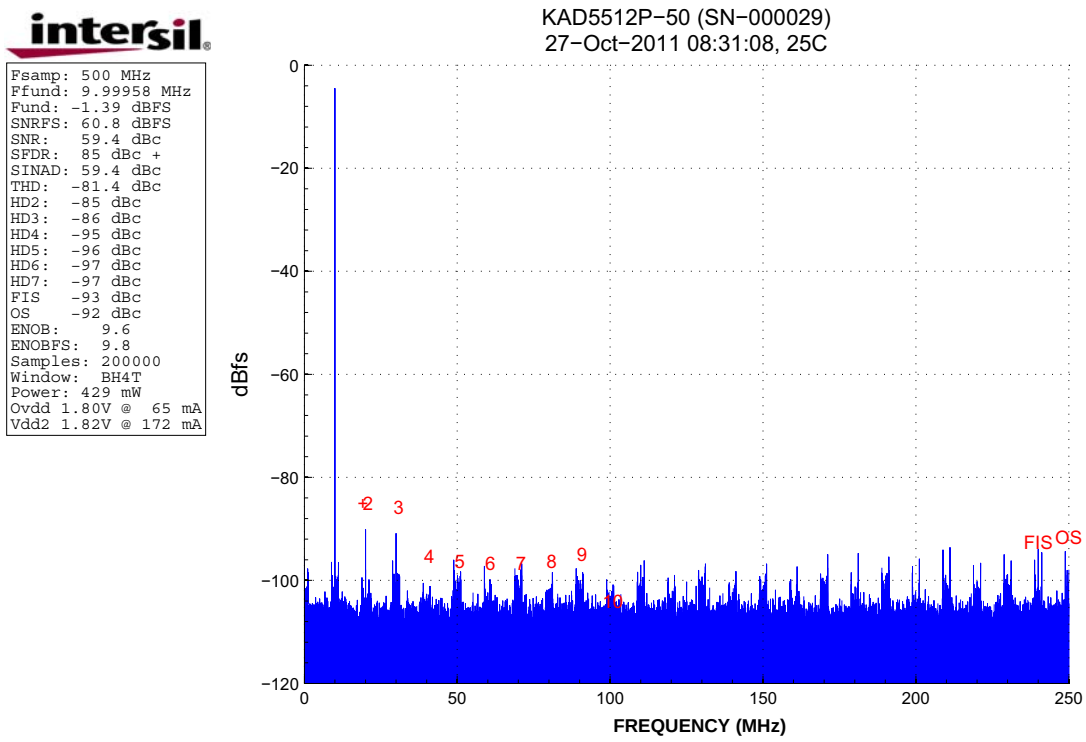

FIGURE 4. KAD5512P-50Q72 IN 10-BIT OUTPUT MODE (EMULATING KAD5510P-50Q72)